PENDING CLAIMS AND STATUS THEREOF

1. **(currently amended)**: A system using current pulses having controlled **constant** amplitudes and pulse-widths for charging columns of a liquid crystal display to voltages representative of pixel gray scale shades, said system comprising:

a liquid crystal display (LCD) having a matrix of liquid crystal pixels, said matrix comprising a plurality of columns and a plurality of rows, wherein an intersection of a row and a column defines a location of a pixel;

at least one digital-to-analog converter (DAC) adapted to receive digital inputs representative of ~~amplitudes of~~ **constant** current ~~pulses~~ **amplitudes** and having an output of the **constant** current ~~pulse~~ amplitudes; and

a pulse-width control circuit coupled between the output of said at least one DAC and the plurality of columns of said LCD, wherein the pulse-width control circuit determines pulse-widths **[[of]] for a plurality of current pulses having** the **constant** current ~~pulse~~ amplitudes**, whereby [[and]]** each of the ~~amplitude and pulse-width controlled~~ **plurality of** current pulses are used to charge respective ones of said plurality of columns to voltages representing pixel gray scale shades.

2. (original): The system of claim 1, wherein a plurality of row switches selectively couples said matrix of pixels to said plurality of columns.

3. (original): The system of claim 2, wherein a plurality of column switches selectively couples the output of said at least one DAC to each of said plurality of columns.

4. (original): The system of claim 3, wherein column control logic controls said plurality of column switches and row control logic controls said plurality of row switches.

5. (original): The system of claim 4, further comprising an LCD pixel matrix address controller adapted for controlling said column and row control logic.

6. (original): The system of claim 5, further comprising a video frame to LCD pixel matrix address logic coupled to said LCD pixel matrix address controller, said video frame to LCD pixel matrix address logic adapted to receive video information and generate LCD pixel matrix addresses for said LCD pixel matrix address controller.

7. (previously presented): The system of claim 1, further comprising a gray scale current pulse look-up table adapted for converting said pixel gray scale shades into the digital inputs received by said at least one DAC.

8. (original): The system of claim 7, further comprising a gray scale conversion logic coupled to said gray scale current pulse look-up table.

9. (previously presented): The system of claim 8, wherein said gray scale conversion logic is adapted to receive video information and generate said pixel gray scale shades for said gray scale conversion logic.

Claim 10 (previously canceled)

11. (previously presented): The system of claim 1, wherein said pulse-width control circuit is coupled to a gray scale current pulse look-up table.

12. (previously presented): The system of claim 1, wherein said pulse-width control circuit is synchronized with a column clock.

13. (previously presented): The system of claim 12, further comprising a phase-locked-loop (PLL) coupled between the column clock and a clock input to said pulse-width control circuit, wherein said PLL is adapted to synchronize said clock input with said column clock.

14. (previously presented): The system of claim 13, wherein said PLL generates said clock input to said pulse-width control circuit.

15. (original): The system of claim 1, further comprising an analog-to-digital converter (ADC) for converting said voltages on said columns to digital voltage values.

16. (previously presented): The system of claim 15, further comprising a digital comparator for comparing said voltages representing said pixel gray scale shades with said digital voltage values from said ADC.

17. (previously presented): The system of claim 16, wherein comparisons of said voltages representing said pixel gray scale shades with said digital voltage values are used in determining compensation coefficients for each of said plurality of columns having different capacitance values.

18. (original): The system of claim 17, further comprising a memory for storing said compensation coefficients.

19. (original): The system of claim 1, wherein each of said plurality of columns has substantially the same capacitance.

20. (original): The system of claim 1, wherein each of said plurality of columns is compensated to have substantially the same capacitance.

21. (original): The system of claim 20, further comprising at least one capacitor connected to some ones of said plurality of columns such that each of said plurality of columns has substantially the same capacitance as another column.

22. (original): The system of claim 21, further comprising a column capacitance compensation circuit and at least one switch for coupling said at least one capacitor to said some ones of said plurality of columns.

23. (original): The system of claim 22, further comprising a column capacitance compensation memory coupled to said column capacitance compensation circuit, said column capacitance compensation memory storing connection setting for said at least one switch for coupling said at least one capacitor to said some ones of said plurality of columns.

24. (original): The system of claim 21, wherein said at least one capacitor is a plurality of capacitors having capacitance values in a binary progression.

25. (original): The system of claim 1, wherein said LCD is fabricated on a semiconductor integrated circuit.

26. (original): The system of claim 25, wherein said at least one DAC is fabricated on said semiconductor integrated circuit.

27. (original): The system of claim 3, wherein said plurality of column switches and said plurality of row switches are fabricated on a semiconductor integrated circuit.

28. (original): The system of claim 4, wherein said column control logic and said row control logic are fabricated on a semiconductor integrated circuit.

29. (original): The system of claim 5, wherein said LCD pixel matrix address controller is fabricated on a semiconductor integrated circuit.

30. (original): The system of claim 6, wherein said video frame to LCD pixel matrix address logic is fabricated on a semiconductor integrated circuit.

31. (original): The system of claim 7, wherein said gray scale current pulse look-up table is fabricated on a semiconductor integrated circuit.

32. (original): The system of claim 8, wherein said gray scale conversion logic is fabricated on a semiconductor integrated circuit.

33. (previously presented): The system of claim 1, wherein said pulse-width control circuit is fabricated on a semiconductor integrated circuit.

34. (original): The system of claim 11, wherein said gray scale current pulse look-up table is fabricated on a semiconductor integrated circuit.

35. (original): The system of claim 16, wherein said comparator and said ADC are fabricated on a semiconductor integrated circuit.

36. (original): The system of claim 22, wherein said column capacitance compensation circuit and said at least one switch are fabricated on a semiconductor integrated circuit.

37. **(currently amended)**: An apparatus for generating current pulses having **constant** ~~**controlled**~~ amplitudes ~~**and pulse-widths**~~ that charge columns of a liquid crystal display to voltages representative of pixel gray scale shades, said apparatus comprising:

at least one digital-to-analog converter (DAC) adapted to receive digital inputs representative of ~~**amplitudes of**~~ **constant** current ~~**pulses**~~ **amplitudes** and having an output of the **constant** current ~~**pulse**~~ amplitudes; and

a pulse-width control circuit coupled to the output of said at least one DAC and adapted for coupling to a plurality of columns of a liquid crystal display (LCD), the LCD comprises a matrix of liquid crystal pixels, said matrix comprising a plurality of columns and a plurality of rows, and an intersection of a row and a column defines a location of a pixel, wherein the pulse-width control circuit determines pulse-widths **[[of]]** **for a plurality of current pulses having** the **constant** current ~~**pulse**~~ amplitudes**, whereby [[and]]** each of the ~~**amplitude and pulse-width controlled**~~ **plurality of** current pulses are used to charge respective ones of the plurality of columns to voltages representing pixel gray scale shades.

38. (previously presented): The apparatus of claim 37, further comprising a gray scale current pulse look-up table adapted for converting said pixel gray scale shades into the digital inputs received by said at least one DAC.

39. (previously presented): The apparatus of claim 38, further comprising a gray scale conversion logic coupled to said gray scale current pulse look-up table.

40. (previously presented): The apparatus of claim 39, wherein said gray scale conversion logic is adapted to receive video information and generate said pixel gray scale shades for said gray scale conversion logic.

Claim 41 (previously canceled):

42. (previously presented): The apparatus of claim 37, wherein said pulse-width control circuit is coupled to a gray scale current pulse look-up table.

43. (previously presented): The apparatus of claim 37, wherein said pulse-width control circuit is synchronized with a column clock.

44. (previously presented): The apparatus of claim 43, further comprising a phase-locked-loop (PLL) coupled between the column clock and a clock input to said pulse-width control circuit, wherein said PLL is adapted to synchronize said clock input with said column clock.

45. (previously presented): The apparatus of claim 44, wherein said PLL generates said clock input to said pulse-width control circuit.

46. (previously presented): The apparatus of claim 37, further comprising a comparator circuit for comparing said voltages representing said pixel gray scale shades with said voltages from said ADC.

47. (previously presented): The apparatus of claim 46, wherein comparisons of said voltages representing said pixel gray scale shades with said voltage are used in determining

compensation coefficients for each of said plurality of columns having different capacitance values.

48. (previously presented): The apparatus of claim 47, further comprising a memory for storing said compensation coefficients.

49. **(currently amended)**: A method using current pulses having controlled **constant** amplitudes and pulse-widths for charging columns of a liquid crystal display (LCD) to voltages representative of pixel gray scale shades, said method comprising the steps of:

providing a liquid crystal display (LCD) having a matrix of liquid crystal pixels, said matrix comprising a plurality of columns and a plurality of rows, wherein an intersection of a row and a column defines a location of a pixel; and

charging each of said plurality of columns to voltages representing pixel gray scale shades with current pulses having controlled **constant** amplitudes and pulse-widths representative of the pixel gray scale shades.

50. (original): The method of claim 49, wherein the current controlled charging circuit is a current output digital-to-analog converter (DAC).

51. (original): The method of claim 49, further comprising the step of selectively coupling said matrix of pixels to said plurality of columns.

52. (original): The method of claim 49, wherein the step of charging is done with current pulses.

Claims 53 and 54 (previously canceled)

55. (previously presented): The method of claim 49, wherein the pulse-widths are determined with a gray scale current pulse look-up table.

56. (original): The method of claim 49, further comprising the step of measuring the voltages on said plurality of columns.

57. (previously presented): The method of claim 56, further comprising the step of comparing the voltages representing the pixel gray scale shades with the voltages measured on said plurality of columns.

58. (previously presented): The method of claim 57, further comprising the step of determining compensation coefficients from differences between the voltages representing the pixel gray scale shades and the voltages measured on said plurality of columns for each of said plurality of columns.

59. (original): The method of claim 58, further comprising the step of storing the compensation coefficients in a memory.

60. (original): The method of claim 49, further comprising the step of adding compensating capacitance to said plurality of columns such that each of said plurality of columns has substantially the same capacitance as the others.

61. (original): The system of claim 1, further comprising a circuit for setting said plurality of columns to a desired voltage before charging said plurality of columns to said voltages.

62. (original): The system of claim 61, wherein the desired voltage is substantially zero.

63. (original): The system of claim 1, further comprising a circuit for discharging said plurality of columns before charging said plurality of columns to said voltages.

64. (previously presented): The system of claim 1, further comprising a comparison circuit for comparing said voltages representing said pixel gray scale shades with said voltages on said columns, said comparison circuit output being used in determining compensation coefficients for each of said plurality of columns having different capacitance values.

65. (original): The system of claim 20, wherein each of said plurality of columns is compensated with a fuse link connected plurality of capacitors.

66. (original): The method of claim 60, wherein the step of adding compensating capacitance to said plurality of columns comprises the steps of blowing fuse links connected to a plurality of compensation capacitors.